

# CBCS SCHEME

SVKM's Institute of Technology  
Library, Mangalore

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17ELN15/25

## First/Second Semester B.E. Degree Examination, July/August 2022 Basic Electronics

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- Explain the V-I characteristics of p-n junction diode. (08 Marks)
  - With neat circuit diagram and waveform explain the working of full wave bridge rectifier. (08 Marks)
  - Derive the relationship between  $\alpha$  and  $\beta$ . Also calculate the  $\alpha$  value and  $\beta$  value of a transistor. If  $I_{\beta} = 100\mu\text{A}$  and  $I_C = 2\text{mA}$ . (04 Marks)

OR

- With a neat diagram, explain the Input-Output characteristics of a transistor in common base configuration. (08 Marks)
  - With neat circuit diagram and waveforms, explain the working of a half-wave rectifier. (08 Marks)
  - Explain briefly capacitor filter circuit. (04 Marks)

### Module-2

- Explain the characteristic of Ideal operational amplifier. (06 Marks)
  - What is DC load line? Explain with neat circuit the operation of voltage divider bias circuit. (08 Marks)
  - Derive the output expression of Op-Amp differentiator. (06 Marks)

OR

- Calculate the output voltage of a three input inverting summing amplifier, given  $R_1 = 200\text{K}\Omega$ ,  $R_2 = 250\text{K}\Omega$ ,  $R_3 = 500\text{K}\Omega$ ,  $R_f = 1\text{M}\Omega$ ,  $V_1 = -2\text{V}$ ,  $V_2 = -1\text{V}$  and  $V_3 = +3\text{V}$ . (06 Marks)
  - For the circuit shown in Fig.Q.4(b) find the Q-point values and draw DC-load line, where  $V_{BE} = 0.7\text{V}$  and  $\beta = 50$ . (06 Marks)

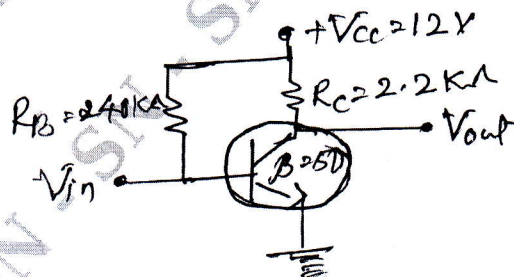


Fig.Q.4(b)

- Explain briefly inverting and non-inverting operational amplifiers. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

**Module-3**

- 5 a. Convert:
- $(1101101)_2 = (?)_{10}$  and  $(101.01)_2 = (?)_{10}$
  - $(48350)_{10} = (?)_{16} = (?)_8$
  - $(FA876)_{16} = (?)_8 = (?)_{10}$
  - $(237)_8 = (?)_{16} = (?)_{10}$ . (08 Marks)
- b. Perform the subtraction:
- $(22 - 17)_{10}$  by using 1's complement. (04 Marks)
  - $(11010)_2 - (10000)_2$  by using 2's complement. (08 Marks)
- c. State and prove De-Morgan's theorems. (08 Marks)

**OR**

- 6 a. Explain the full adder circuit with circuit diagram, truth table. (05 Marks)
- b. What are universal gates? Realize AND and OR gates using NAND gates. (05 Marks)
- c. Simplify:  $y = \overline{ABCD} + \overline{AB}CD + \overline{ABC}D + \overline{ABC}D$ . (05 Marks)
- d. Draw and explain half adder circuit. (05 Marks)

**Module-4**

- 7 a. Explain the operation of NOR Latch with symbol, circuit diagram and truth table. (06 Marks)
- b. Explain with neat block diagram architecture of 8051 microcontroller. (08 Marks)
- c. Explain the working of clocked RS-flip flop using NAND-gates. (06 Marks)

**OR**

- 8 a. Write a note on NAND-gate latch. (06 Marks)
- b. With the help of block diagram, explain the microcontroller based stopper motor control system. (08 Marks)
- c. Explain R-S flip-flop with diagram and truth table. (06 Marks)

**Module-5**

- 9 a. With the help of block diagram, explain the communication system. (06 Marks)
- b. Define Modulation. Derive mathematical expression for amplitude modulation, draw waveforms. (06 Marks)
- c. Explain the construction and working principle of LVDT. (08 Marks)

**OR**

- 10 a. A carrier of 1MHz, with 400W of its power is amplitude modulated with a sinusoidal signal of 2500Hz. The depth of modulation is 75%. Calculate the side band frequency, Bandwidth, the power in the side bands and the total power in the modulated wave. (06 Marks)
- b. List the differences between Amplitude Modulation and frequency modulation. (06 Marks)
- d. Explain the piezoelectric transducer and photo electric transducer. (08 Marks)

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